



## Prospects for SiGe thermoelectric generators



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### ABSTRACT

Thermoelectric materials are one potential technology that could be used for energy harvesting. Here we report results from nanoscale Ge/SiGe heterostructure materials grown on Si substrates designed to enhance the thermoelectric performance over bulk materials at room temperature. The materials and devices are aimed at integrated energy harvesters for autonomous sensing applications. We report Seebeck coefficients up to  $279.5 \pm 1.2 \mu\text{V/K}$  at room temperature with electrical conductivities of  $77,200 \text{ S/m}$  which produce a high power factor of  $6.02 \pm 0.05 \text{ mW m}^{-1} \text{ K}^{-2}$  and a ZT of  $0.135 \pm 0.074$  at room temperature. Methods for microfabricating modules will be described along with the first demonstration of power output from flip-chip bonded SiGe legs.

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## 1. Introduction

The generation of electricity from thermal energy through the Seebeck effect has renewed interest for a range of applications including industrial energy harvesting, replacing car alternators to improve automotive fuel consumption and to power autonomous sensors [1]. For many sensing applications, sensors require lifetimes of tens of years and the cost of replacing batteries is orders of magnitude greater than the cost of the system. Energy harvesters such as thermoelectrics could potentially allow fit and forget solutions where the battery never needs to be replaced or indeed the battery may be completely removed from the system.

The figure of merit for thermoelectric materials is defined as

$$ZT = \frac{\alpha^2 \sigma}{\kappa} T \quad (1)$$

where  $\alpha$  is the Seebeck coefficient,  $\sigma$  is the electrical conductivity,  $T$  is the temperature and  $\kappa$  is the thermal conductivity [1]. The best thermoelectric materials for room temperature operation at present are based on bulk  $\text{Bi}_2\text{Te}_3$  and  $\text{Sb}_2\text{Te}_3$  with  $ZT \approx 1$  but tellurium is one of the rarest elements on the planet and there is great demand for a sustainable replacement [1,2]. The maximum power that can be delivered to a load is related to the power factor,  $\alpha^2 \sigma$  so this parameter must also be optimised for practical systems. More

importantly, when the temperature drop across the material is small (i.e. for  $\Delta T < 25 \text{ K}$ ) and the output power is more important than the efficiency, a high power factor can produce significantly more output power from better electrical and thermal impedance matching than the optimization of ZT.

A large ZT requires a high electrical conductivity and a low thermal conductivity. Due to the Wiedemann–Franz rule, the two are proportional to each other in bulk 3D materials and it is therefore difficult to engineer enhanced thermoelectric materials [2]. It is possible to engineer structures in which there are weaker relationships between the electrical and thermal conductivities by using low dimensional nanostructured materials. The Seebeck coefficient can be engineered using [3]

$$\alpha = -\frac{\pi^2}{3q} k_B^2 T \left[ \frac{d \ln (\mu(E)g(E))}{dE} \right] \Big|_{E=E_F} \quad (2)$$

where  $q$  is the electron charge,  $k_B$  is Boltzmann's constant,  $\mu$  is the mobility,  $g$  is the density of states,  $E$  is the energy and  $E_F$  is the Fermi energy. Therefore the use of quantum wells, 1D or 0D nanostructures can also enhance the Seebeck coefficient through the enhancement of the density of states [3,4].

The approach reported in this paper uses Ge/SiGe heterostructures on Si substrates to produce quantum wells and quantum dots which have previously demonstrated high ZTs at high temperatures [5] and can be easily integrated onto silicon chips through back-end-of-line processing. Nanofabrication is also being used

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to etch 1D nanowires of Ge/SiGe heterostructures to investigate further potential enhancements. In this paper lateral structures using Ge quantum wells will be investigated with the aim of improving the ZT and power factor of SiGe material compared to bulk values.

## 2. Fabrication

The SiGe heterolayers were grown using low energy plasma enhanced chemical vapor deposition (LEPECVD) [6] which has previously demonstrated high quality Ge/SiGe superlattices for electrical and optical applications [7]. The technique allows high quality quantum wells and barriers to be grown with relatively high growth rates which is essential for the thick (10  $\mu\text{m}$  plus) superlattice stacks required for thermoelectric applications. The heterolayers were grown on top of 100 mm silicon-on-insulator (SOI) substrates with a thin strain relaxation buffer and the quantum wells and barriers strain symmetrised to prevent strain relaxation of the thick stack [8].

Two different designs of material were grown and compared [9,10]. Design 1 consisted of 378 repeats of a 9 nm i-Ge QW, 5 nm i- $\text{Si}_{0.3}\text{Ge}_{0.7}$  spacer, 7.5 nm p- $\text{Si}_{0.3}\text{Ge}_{0.7}$  supply layer ( $N_A = 1 \times 10^{19} \text{ cm}^{-3}$ ) and a 5 nm i- $\text{Si}_{0.3}\text{Ge}_{0.7}$  spacer all grown on a  $\text{Si}_{0.2}\text{Ge}_{0.8}$  relaxed buffer layer. The surface of the superlattice was capped with a 5 nm i- $\text{Si}_{0.3}\text{Ge}_{0.7}$  spacer, a 7.5 nm p- $\text{Si}_{0.3}\text{Ge}_{0.7}$  supply layer ( $N_A = 1 \times 10^{19} \text{ cm}^{-3}$ ), a 5 nm i- $\text{Si}_{0.3}\text{Ge}_{0.7}$  spacer, a 30 nm i- $\text{Si}_{0.2}\text{Ge}_{0.8}$  spacer and a 4 nm i-Si cap. Design 2 consisted of 378 repeats of a 9 nm i-Ge QW, 5 nm i- $\text{Si}_{0.4}\text{Ge}_{0.6}$  spacer, 7.66 nm p- $\text{Si}_{0.4}\text{Ge}_{0.6}$  supply layer ( $N_A = 1 \times 10^{19} \text{ cm}^{-3}$ ) and a 5 nm i- $\text{Si}_{0.4}\text{Ge}_{0.6}$  spacer all grown on a  $\text{Si}_{0.25}\text{Ge}_{0.75}$  relaxed buffer layer. The surface of the superlattice was capped with a 5 nm i- $\text{Si}_{0.4}\text{Ge}_{0.6}$  spacer, a 7.5 nm p- $\text{Si}_{0.4}\text{Ge}_{0.6}$  supply layer ( $N_A = 1 \times 10^{19} \text{ cm}^{-3}$ ), a 5 nm i- $\text{Si}_{0.4}\text{Ge}_{0.6}$  spacer, a 30 nm i- $\text{Si}_{0.25}\text{Ge}_{0.75}$  spacer and a 4 nm i-Si cap. In both cases a 10  $\mu\text{m}$  thick superlattice was chosen so that the active material was approximately 10 times the thickness of the buffer to reduce the electrical and thermal contributions of the buffer and top Si device layer of the SOI.

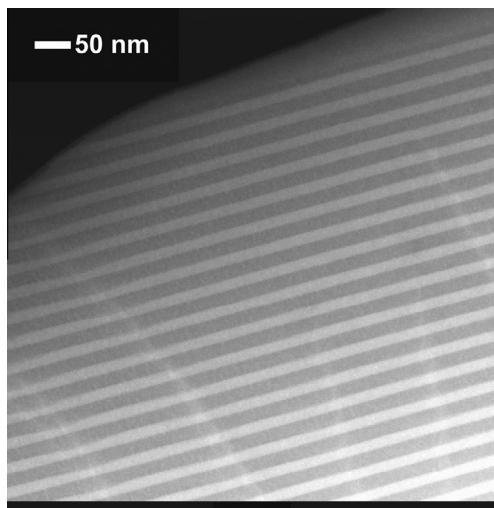
Fig. 1 shows a transmission electron micrograph (TEM) of Ge quantum wells grown on the thin strain relaxation buffer on top of the SOI substrate. Due to the thin virtual substrate, the dislocation density is around  $10^9 \text{ cm}^{-2}$  as measured by planar TEM. X-ray diffraction and TEM [9,11] were used to measure the quantum

well, barrier and superlattice period across the wafer and this is presented in Fig. 2. The variation allows the thermoelectric properties to be determined as a function of quantum well width providing a larger range of data to be characterised.

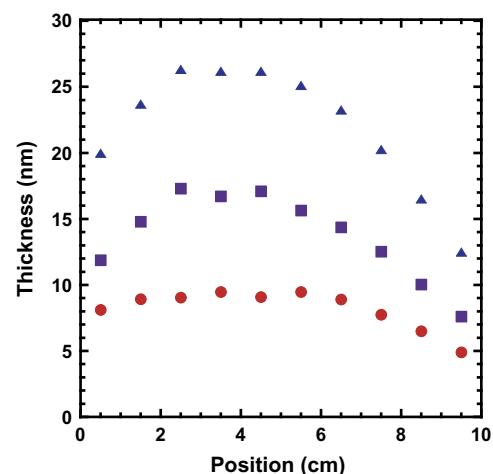
Holes in this design are transported along the quantum wells and so to characterise the material, free standing Hall bars with electrical heaters at each end are required to provide a temperature gradient along the sample. Integrated thermometers and electrical contacts are also fabricated to allow the electrical conductivity, thermal conductivity and Seebeck coefficients to be extracted on a single sample (see Fig. 3). The thermometers consist of 20 nm of Ti with 100 nm of Pt and are calibrated to obtain an accurate temperature coefficient of resistance before being used [12]. The thermal conductivity is particularly difficult to measure and we use a novel technique where the material in the Hall bar is measured before the central part of the Hall bar is cut out leaving the heaters and thermometers. Measurements are then made to obtain the parasitic heat transport down the thermometers and heater leads and this allows an accurate determination of the heat flux which is transported down the material, essential to determine the thermal conductivity with a high level of accuracy [12,11].

## 3. Thermoelectric characterisation

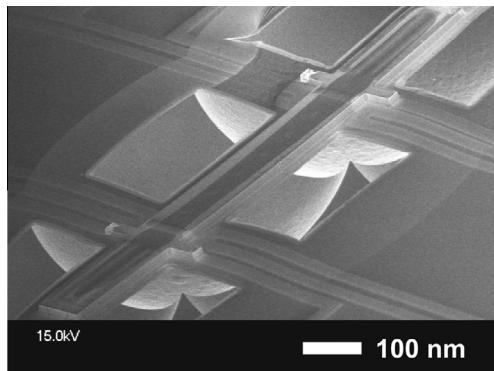
The electrical conductivity was measured on Hall bar samples (see Fig. 3) using a 4 terminal technique to remove all series resistances. The technique allows the electrical conductivity to be measured with an uncertainty below 1% [11]. The electrical conductivity as a function of quantum well width is plotted in Fig. 4. For bulk Ge doped at a comparable level the electrical conductivity is 33,300 S/m [13] and so the modulation doping technique has clearly produced higher values. As the quantum well width is reduced, there is a sudden transition to a reduced electrical conductivity for the design 1 samples which can be attributed to an increase in interface roughness scattering [14]. This is only observed for the samples with a larger amount of Si in the barriers which is why interface roughness is the suggested mechanisms. This spacer layer (the undoped spacer between the doping supply layer and the quantum well) is not a constant and will also decrease for the narrower quantum well. The position of the dopant has not been measured in these samples and so the thickness of the spacer layer between the quantum well and the doping supply



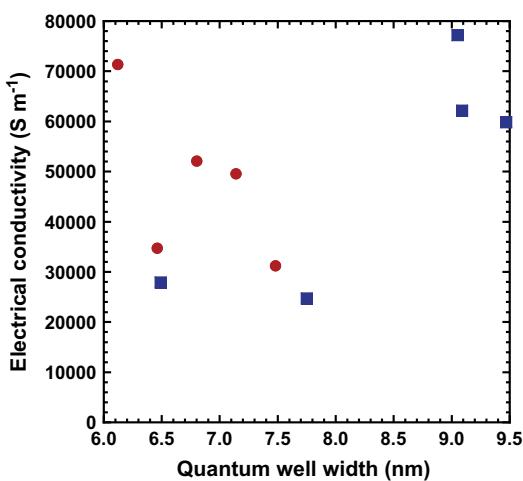
**Fig. 1.** A TEM image of one of the lateral superlattice samples showing Ge quantum wells and SiGe barriers. A number of threading dislocation can be observed to cross the quantum wells.



**Fig. 2.** The quantum well thickness (red circles), barrier thickness (purple squares) and superlattice period (blue triangles) as a function of the radius of the wafer. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)



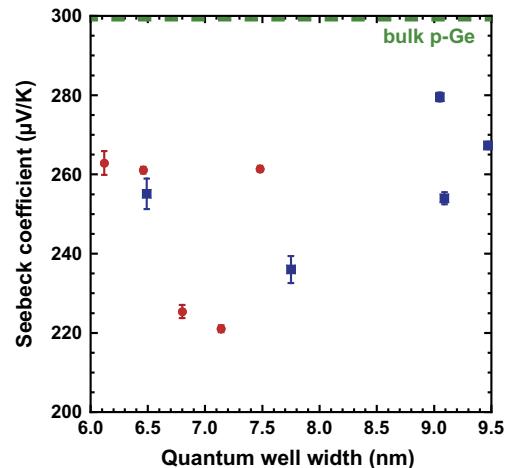
**Fig. 3.** A SEM image of a single free standing Hall bar sample for measuring the electrical conductivity, thermal conductivity and Seebeck coefficient for micro and nanoscale samples.



**Fig. 4.** The electrical conductivity of the samples as a function of quantum well width at 300 K. Design 1 (blue squares), design 2 (red circles). (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

layer is unknown. Whilst the uncertainty in the measurement of electrical conductivity is below 1% of the measured values, the variation observed between the samples is much larger than this value. It is believed that local variations in the high threading dislocation density for each sample results in the variability as the electrical conductivity is very sensitive to the dislocation density in this regime [15].

The Seebeck coefficient was taken as the gradient of the Seebeck voltage versus the temperature difference measured down the length of the Hall bar as a heater at one end created the temperature difference [16]. Fig. 5 demonstrates the variation of the Seebeck coefficient measured as a function of the quantum well width. For this set of samples, the results suggest that the Seebeck coefficient is near constant and it is believed that the small variability in the results is related to local changes in the threading dislocation across the samples being characterized [15]. These results with values between  $236.0 \pm 3.5$  and  $279.5 \pm 1.2 \mu\text{V/K}$  should be compared with a bulk p-type Ge Seebeck coefficient of  $90 \mu\text{V/K}$  at 300 K with comparable doping density of  $\sim 10^{19} \text{ cm}^{-3}$  [17] and thin film p-Ge samples of  $300 \mu\text{V/K}$  [13]. As a high dislocation density can also increase the Seebeck coefficient [15], the present results do not yet demonstrate beyond all reasonable doubt that the enhanced Seebeck coefficient is the result of a larger asymmetry across the chemical potential as suggested by Eq. (1). Further

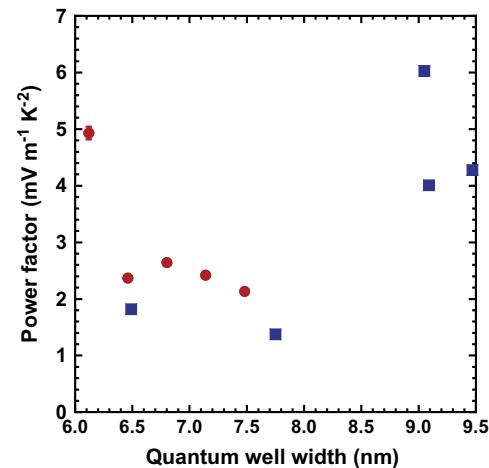


**Fig. 5.** The Seebeck coefficient as a function of quantum well width at 300 K. Design 1 (blue squares), design 2 (red circles). (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

samples with lower dislocation density are required before the true mechanism for the enhanced Seebeck coefficient can be determined.

The power factor as a function of quantum well width has been plotted in Fig. 6. The values need to be compared with bulk p-Ge of  $2.45 \times 10^{-4} \text{ W m}^{-1} \text{ K}^{-2}$  and for thin film p-Ge of  $1.33 \times 10^{-3} \text{ W m}^{-1} \text{ K}^{-2}$ . All the values demonstrate enhancements with the best samples producing power factors six times larger than bulk thin film Ge for a comparable doping density [13].

To obtain the thermal conductivity, a measurement of the heat flux being injected into the hot end of the Hall bar is required [16]. To obtain this, the temperature at each end of the Hall bar was measured using the calibrated thermometers. The Hall bar was then removed allowing the heat that is being transported through parasitic channels such as the electrical, heater and thermometer contacts to the Hall bar to be measured [12,11]. By evaluating how much additional power is required with the Hall bar central section in place to get the hot end of the device to the same temperature, an accurate heat flux being injected into the Hall bar can be extracted. Fourier's law can then be used to calculate the thermal conductivity since the temperature gradient along the Hall bar is known as well as the heat flux entering the Hall bar at the hot



**Fig. 6.** The power factor as a function of quantum well width at 300 K. Design 1 (blue squares), design 2 (red circles). (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

end and the length of the measurement section. Fig. 7 presents the thermal conductivity results from the samples as a function of quantum well width. There is a general trend of lower thermal conductivities for narrower quantum wells for the design 1 samples as would be expected since the diffuse phonon scattering should increase as the quantum well width is reduced. For the design 2 samples with the larger Si content in the barriers, more interface roughness scattering is expected and this will make the phonon scattering less diffuse and more specular resulting in higher thermal conductivity [18–20].

The ZT for the samples as a function of quantum well width is presented in Fig. 8. For bulk Ge, the ZT is  $1.15 \times 10^{-3}$  [17] whilst for thin film Ge it is  $6.23 \times 10^{-3}$ . The present results represent an order of magnitude increase in the ZT figure of merit over bulk Ge demonstrating the benefits of low dimensional structures for improving the ZT. The values, however, are only comparable with the best reported  $\text{Si}_{0.3}\text{Ge}_{0.7}$  results at the same carrier density [21] although the present modulation doped samples have a power factor which is six times larger than the bulk values.

The ZT values are still rather low compared to the best bulk material at 300 K  $\text{Bi}_2\text{Te}_3$ . Initial analysis [22,11] suggests that all the present samples have significant electrical conductivity in the  $\text{Si}_{1-x}\text{Ge}_x$  barriers and therefore optimising the spacer and doping supply layers should allow improved results especially through enhancements to the Seebeck coefficient through the reduced doping. A second issue is that the ZT is strongly dependent on the threading dislocation density for densities above  $10^7 \text{ cm}^{-2}$  [15]. Theory suggests that a reduction of the threading dislocation density to  $10^7 \text{ cm}^{-2}$  or below would increase the ZT by an order of magnitude [15] which would result in ZT values comparable to the best  $\text{Bi}_2\text{Te}_3$  results at room temperature. The power factors are already above bulk  $\text{Bi}_2\text{Te}_3$  at room temperature and these values are expected to improve by a reduction of the threading dislocation density.

#### 4. Thermoelectric modules

To be able to generate electricity, complete thermoelectric modules are required where n- and p-type legs are connected electrically in series and thermally in parallel. For the complete modules it is not just the ZT of the n- and p-type thermoelectric material that effects the performance but also the electrical and thermal contacts to each leg. For a thermoelectric module with  $N$

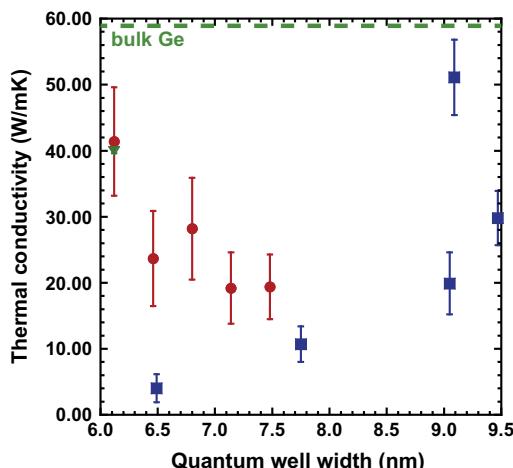


Fig. 7. The thermal conductivity as a function of quantum well width at 300 K. Design 1 (blue squares), design 2 (red circles), design 2 ThAFM (green triangle). (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

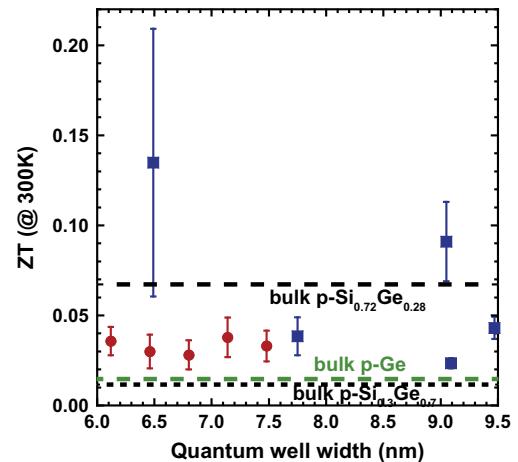


Fig. 8. The ZT as a function of quantum well width at 300 K. Design 1 (blue squares), design 2 (red circles). (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

legs of length,  $L$ , where the specific contact resistivity of the electrical contacts is  $\rho_c$ , the thermal conductivity of the contacts is  $\kappa_c$  and the length of the contacts is  $l_c$ , for a matched electrical load the output power is given by [23]

$$P = \frac{\alpha^2 \sigma A N \Delta T^2}{2(\rho_c \sigma + L) \left(1 + 2 \frac{\kappa l_c}{\kappa_c L}\right)^2} \quad (3)$$

It is clear from this equation that producing materials with high quality electrical contacts is one of the key parameters required to maximise the output power. This is where the SiGe modules may have advantages over other technologies as  $\rho_c$  values below  $1 \times 10^{-8} \Omega \text{ cm}^2$  are available [24].

For complete generators, n- and p-type legs are required to be fabricated on separate wafers and flip-chip bonded together. Fig. 9 demonstrates a test structure to develop the flip-chip bonding process using In bump-bonding and Fig. 10 demonstrates the first output power density from single n- and p-type legs bonded into a complete electrical circuit. The microfabricated module was placed on a hot plate without any cold sink on the top side and so the temperature difference represents the temperature of the hot plate relative to room temperature and therefore overestimates the  $\Delta T$  reported. The powers are relatively low but with optimisation and scaling to large numbers of legs will allow improved performance. As the resistivity of Ohmic contacts to BiTe-alloys presently limits the system output power for microfabricated BiTe-alloy modules, the SiGe technology can potentially have system performance closer to the BiTe than the ZT values suggest since access low access resistance is key for high performance.

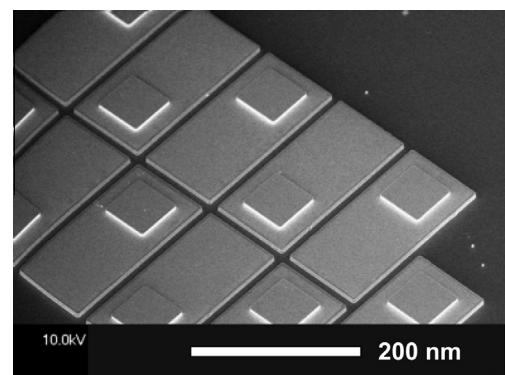
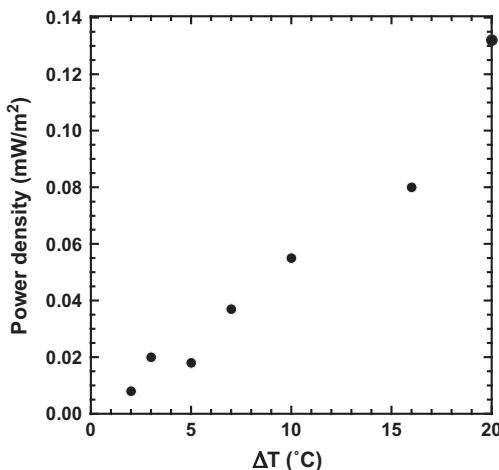


Fig. 9. A SEM image of a module test structure.



**Fig. 10.** The power density versus  $\Delta T$  across one n-type and one p-type SiGe leg in a microfabricated module test structure.

## 5. Conclusion

Enhancements of the Seebeck coefficients, power factors and ZT have been achieved using modulation doped Ge quantum wells grown on Si substrates. Improvements of over an order of magnitude in the power factor and ZT over bulk and thin film Ge has been achieved but the ZT values are presently limited by the threading dislocation density and parallel electrical conduction in the barriers of the device. Modelling suggest that reductions in the threading dislocation density to  $10^7 \text{ cm}^{-2}$  or below would result in an order of magnitude increase in ZT over the present results. Micro-fabricated modules have been demonstrated but still require scaling to more legs and significant optimisation before useful output powers can be delivered.

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